Fig.1

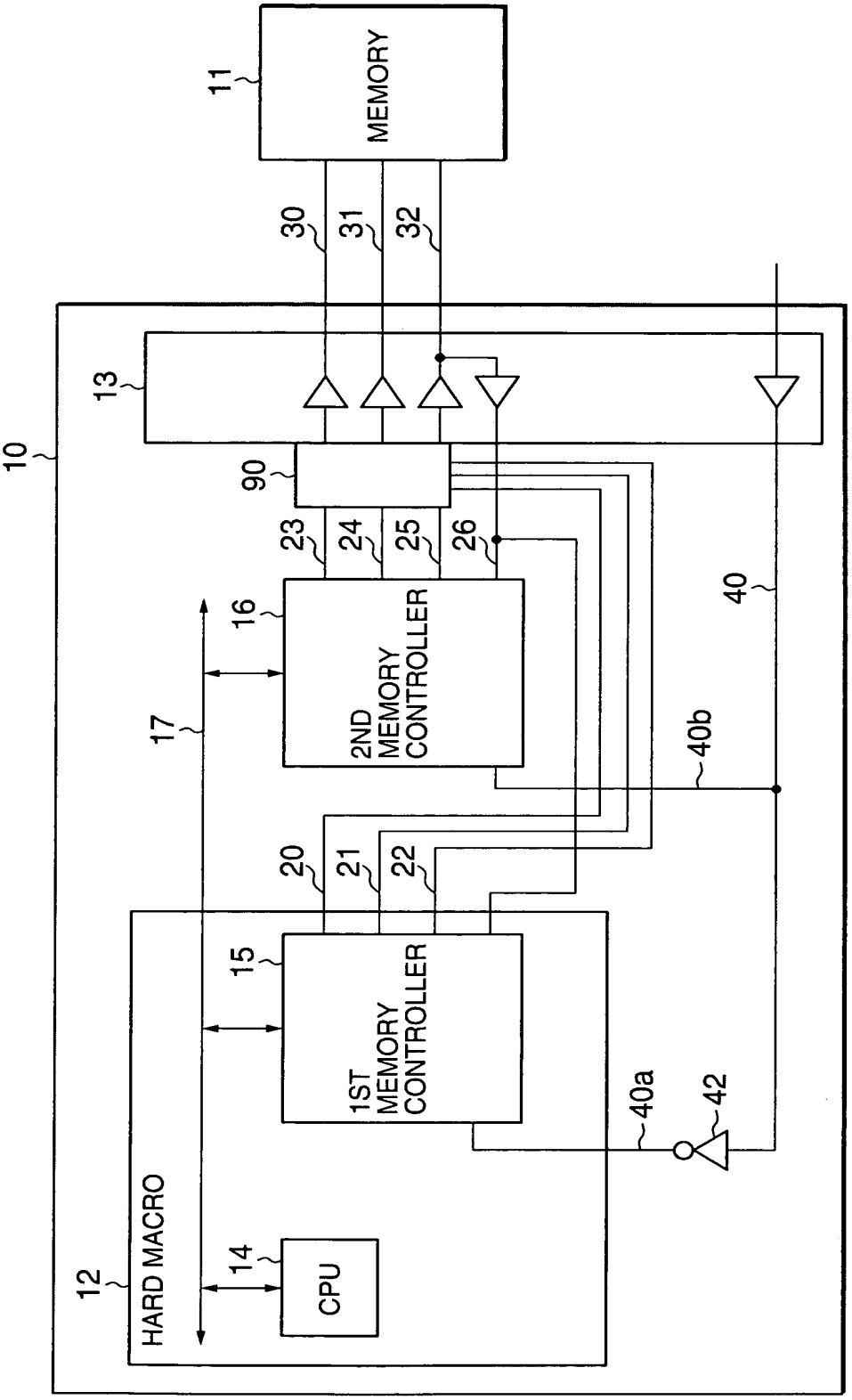

11
MEMORY
30
31
32
10
13
90
23
24
25
26
40
16
2ND MEMORY CONTROLLER
17
40b
20
21
22
15
1ST MEMORY CONTROLLER
40a
42
12
HARD MACRO
14
CPU

Fig.2

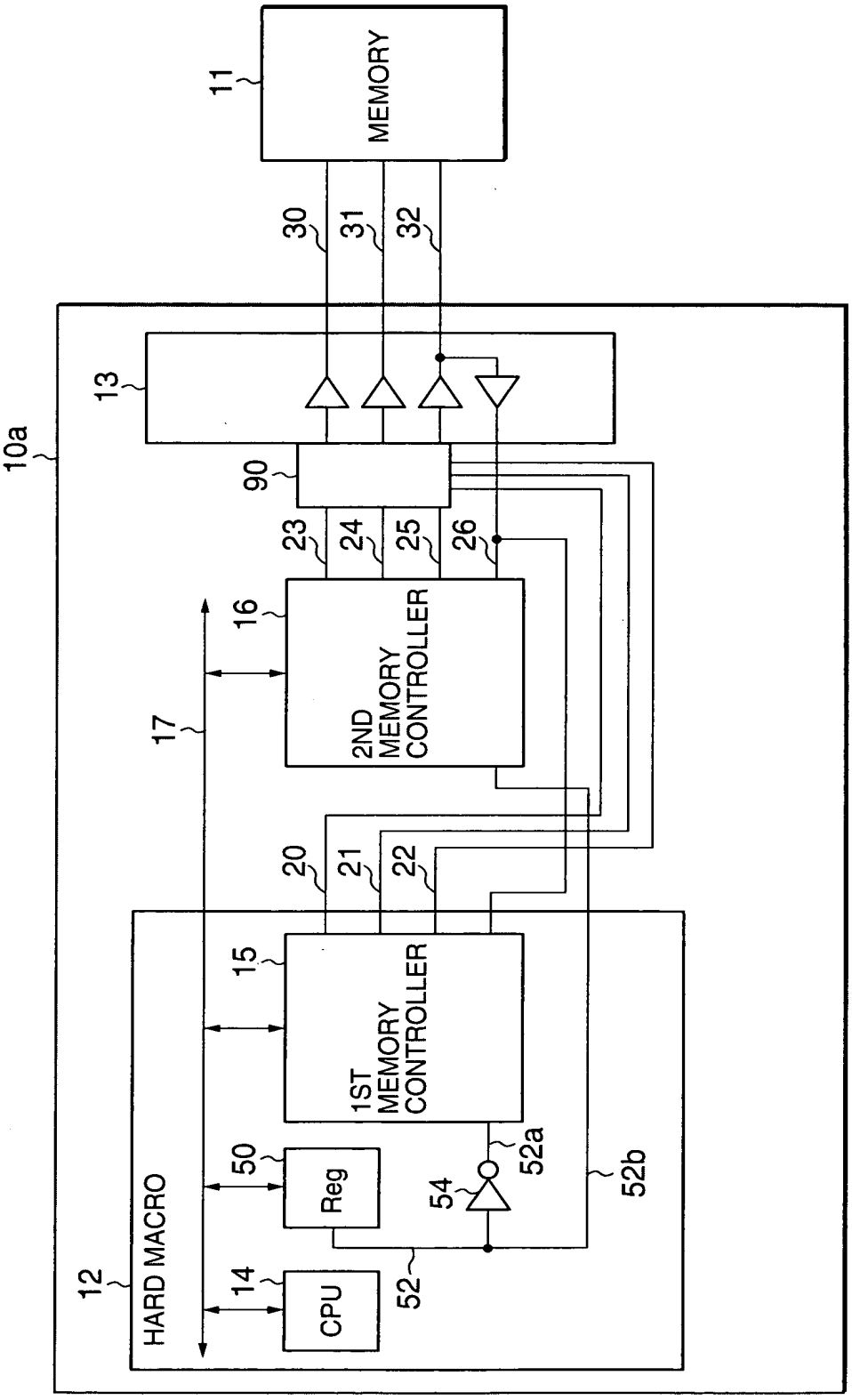

11
MEMORY
30
31
32
10a
13
90
23
24
25
26
16
17
2ND MEMORY CONTROLLER
20
21
22
15
1ST MEMORY CONTROLLER
50
Reg
54
52a
52b
12
HARD MACRO
14
CPU
52

Fig.3

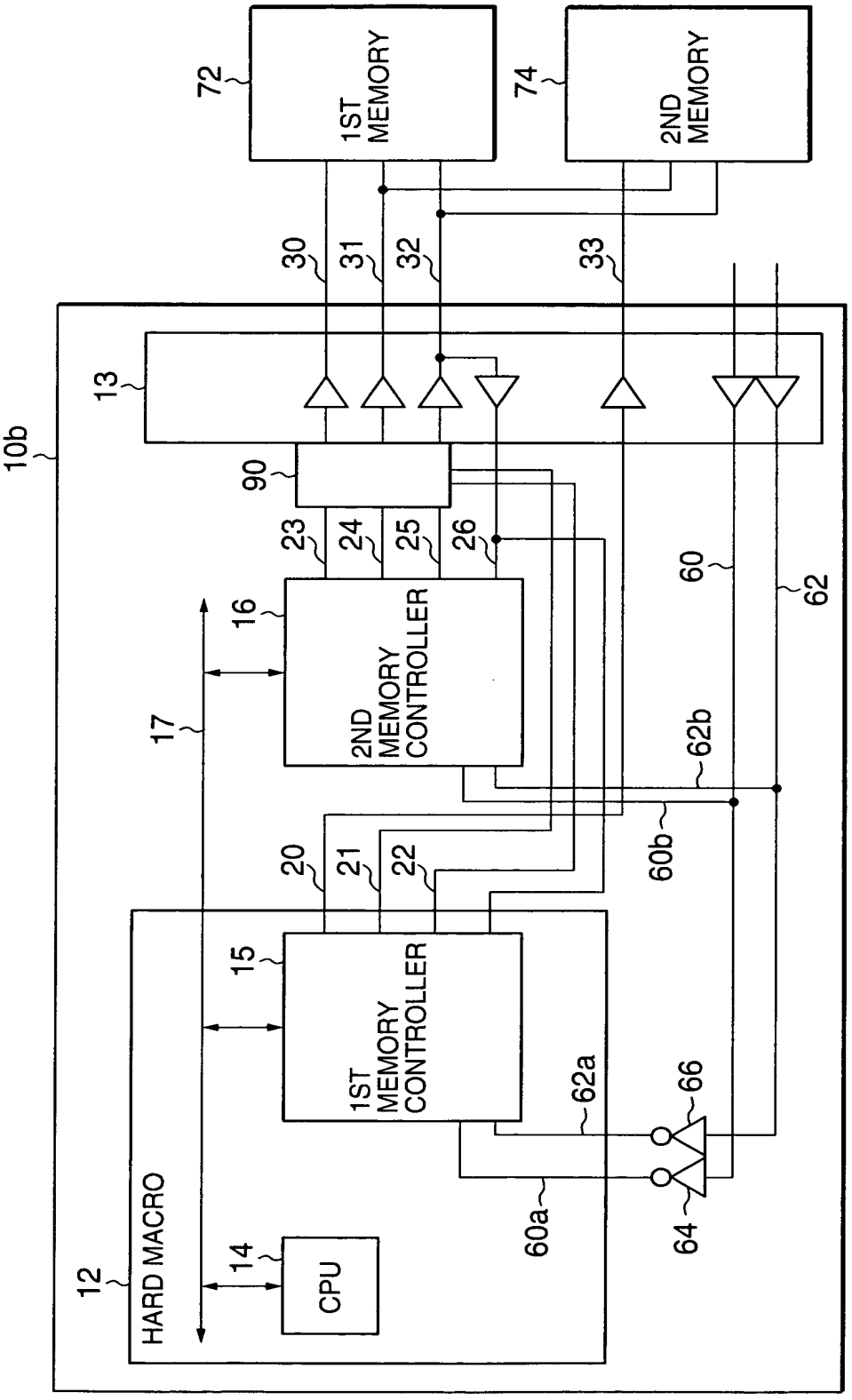

72
1ST MEMORY
74
2ND MEMORY
30
31
32
33
10b
13
90
23
24
25
26
60
62
16
2ND MEMORY CONTROLLER
17
62b
60b
20
21
22
15
1ST MEMORY CONTROLLER
62a
66
60a
64
12
HARD MACRO
14
CPU

Fig.4(A)

(60a)	(62a)	
0	0	:DISABLE
0	1	:LOW
1	0	:HIGH
1	1	:FULL

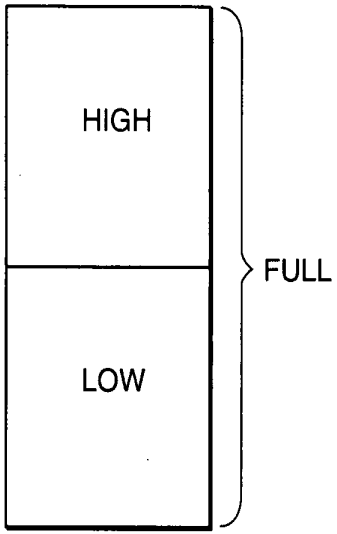
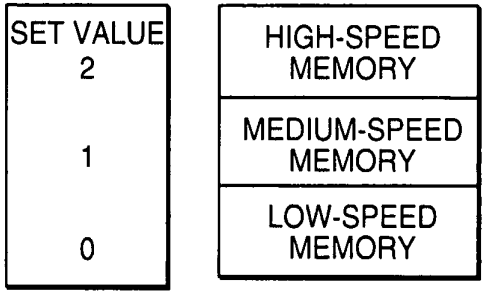


Fig.4(B)

CONTROL REGISTER A
VALID AT LOW&FULL



CONTROL REGISTER B
VALID AT HIGH

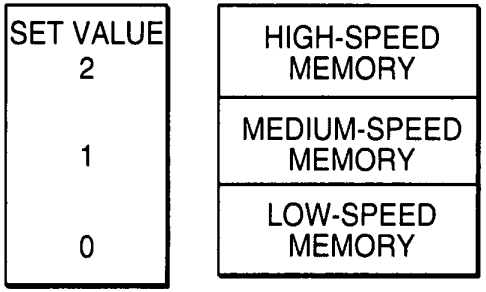


Fig.5

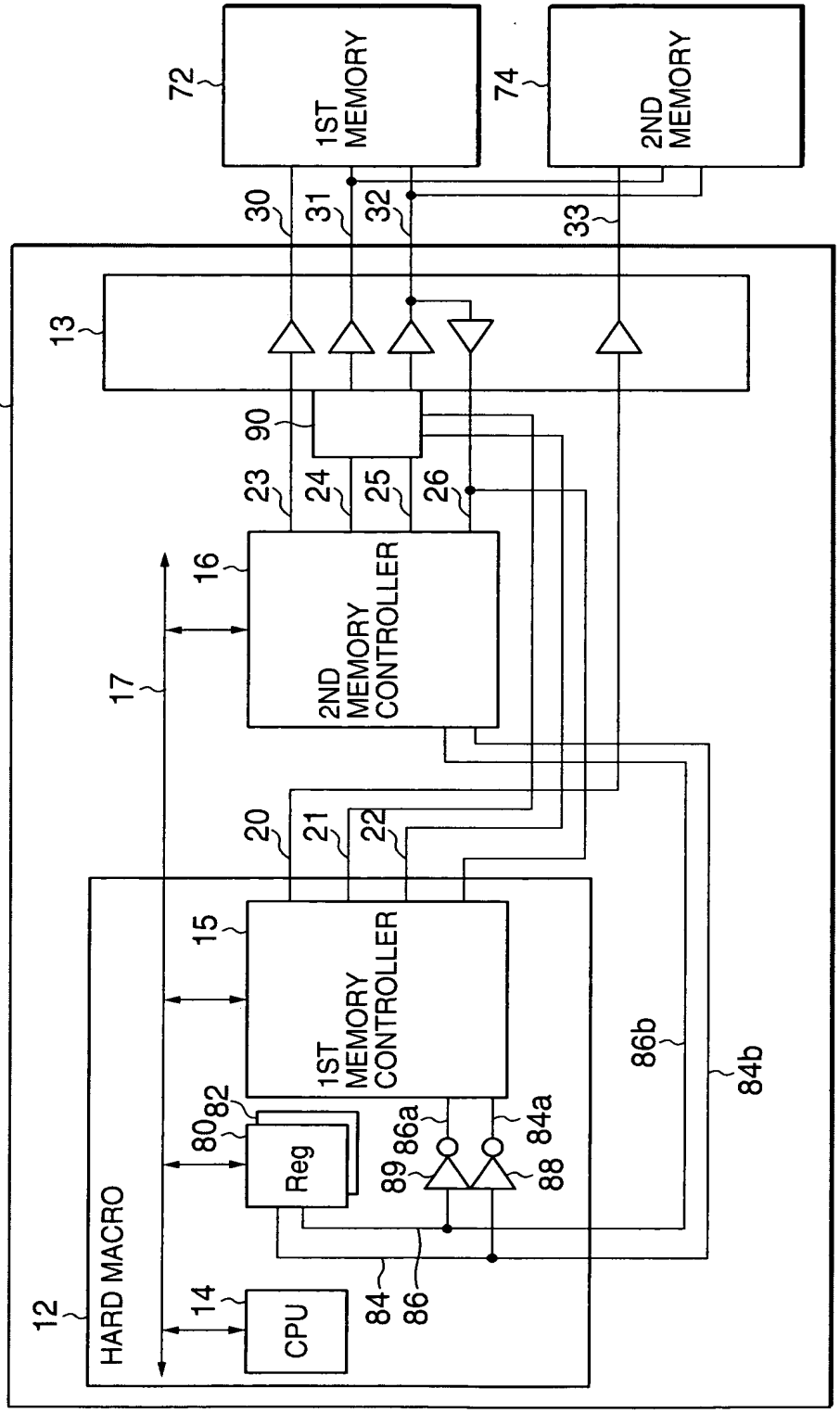
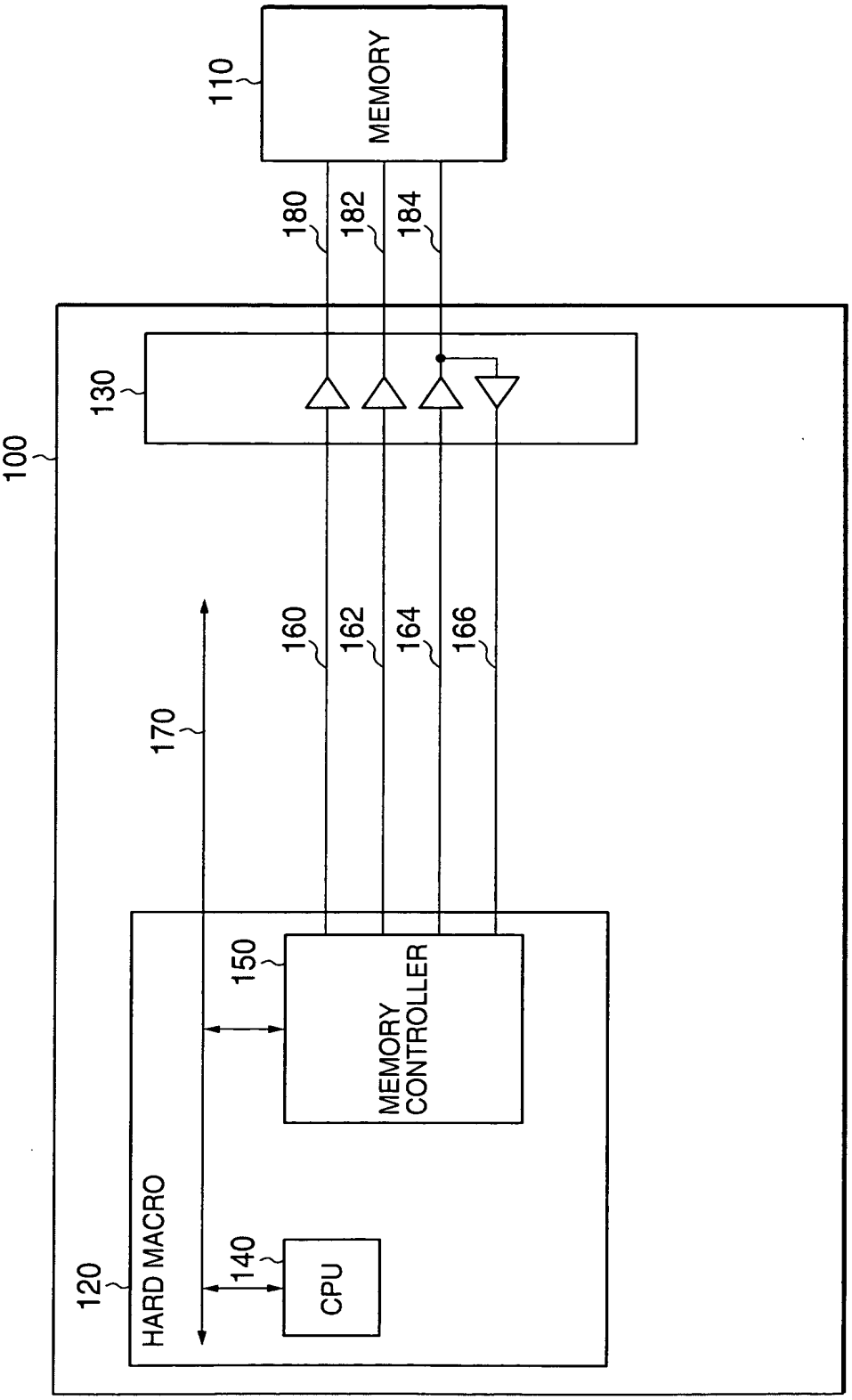

72
1ST MEMORY
74
2ND MEMORY
30
31
32
33
13
10c
90
23
24
25
26
16
2ND MEMORY CONTROLLER
17
20
21
22
15
1ST MEMORY CONTROLLER
86b
84b
80
82
Reg
89
86a
88
84a
12
HARD MACRO
14
CPU
84
86

Fig.6


110
MEMORY
180
182
184
130
100
160
162
164
166
170
150
MEMORY CONTROLLER
120
HARD MACRO
140
CPU